REMARKS

Please charge any required fees and credit any overpayments to Deposit Account No. 502888. Any required extension of time for submitting the present response is hereby requested, if needed.

Claims **1, 24, 30-33,** and **36** were amended to remove the limitation that the hardware description language core interconnection code designates a set of intercore handshake connections and a set of corresponding intercore data connections. New dependent claims **44-50** reciting that limitation were added.

Claims **1-4, 8-24,** and **26-33** and **36-43** were rejected under 35 U.S.C. 103(a) as being unpatentable over Hasley et al. (USPN 5,892,682) in view of Dangelo et al. (USPN 5,493,508) and further in view of Navabi, "VHDL: Analysis and Modeling of Digital Systems."

Applicants thank the Examiner for indicating the allowability of the subject matter of claims **5-7** and **25**. Applicants also thank the Examiner for withdrawing the grounds of rejection set forth in the previous Office Action. The Examiner's rejections are traversed below.

35 U.S.C. §103

The Office Action states that "Dangelo demonstrated that it was known at the time of invention to utilize circuit design system, which provide both software modeling (column 3, lines 55-59) and hardware modeling (column 3, lines 45-54) of cores/modules interchangeably (column 3, lines 60-61). It would have been obvious [...] to implement the modular circuit design of Hasley with modeling in both software and hardware descriptions as found in Dangelo's teaching and thus generate interconnection code for both (hardware and software models) to fulfill modeling of the circuit as previously discussed by Hasley. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide a well defined design of a modular circuit design (Dangelo: column 3, lines 33-45)."

Applicants respectfully submit that the Office Action has not established a *prima facie* case of unpatentability for the present claims, because it is not clear how or why the motivation(s) set

forth by the Office Action would have led one of ordinary skill in the art to arrive at the subject matter of the present claims, which require generating hardware description language and software language models of the circuit according to the same high-level specification.

It is not clear how or why a skilled artisan motivated to provide a well-defined design of a modular circuit design, or motivated to fulfill modeling of the circuit as described by Hasley et al., would have chosen to generate the hardware language and software language models according to the same high-level specification. The Office Action has not pointed out a suggestion or motivation in either Hasley et al. or Dangelo et al. for generating both a hardware model and a software language model according to the same high-level specification. In particular, the Office Action has not pointed out how or why a skilled artisan would have chosen to generate hardware language interconnection code as claimed according to a hierarchy of behavioral models as described by Hasley et al. It is not clear how the fact that it is possible to translate behavioral VHDL code into structural VHDL code as taught by Dangelo et al. provides a suggestion or motivation to generate both a hardware model and a software model according to the same high-level specification.

In light of the above, Applicants respectfully submit the instant claims to be patentable in view of the prior art of record, and request the Examiner to indicate the allowability of the instant claims in the next Office Action.

Respectfully submitted, Date: 5/17/2004

Andrei D. Popovici
Reg. No. 42,401

786 La Mesa Dr., Portola Valley, CA 94028
Tel: (650) 233-1898, Fax: (650) 233-9633
Email: andrei@apatent.com